QV185FHB-N81

Product Specification

Rev. P0

FUZHOU BOE OPTOELECTRONICS TECHNOLOGY Co.,LTD

REVISION HISTORY

(√)preliminary specification

( )Final specification

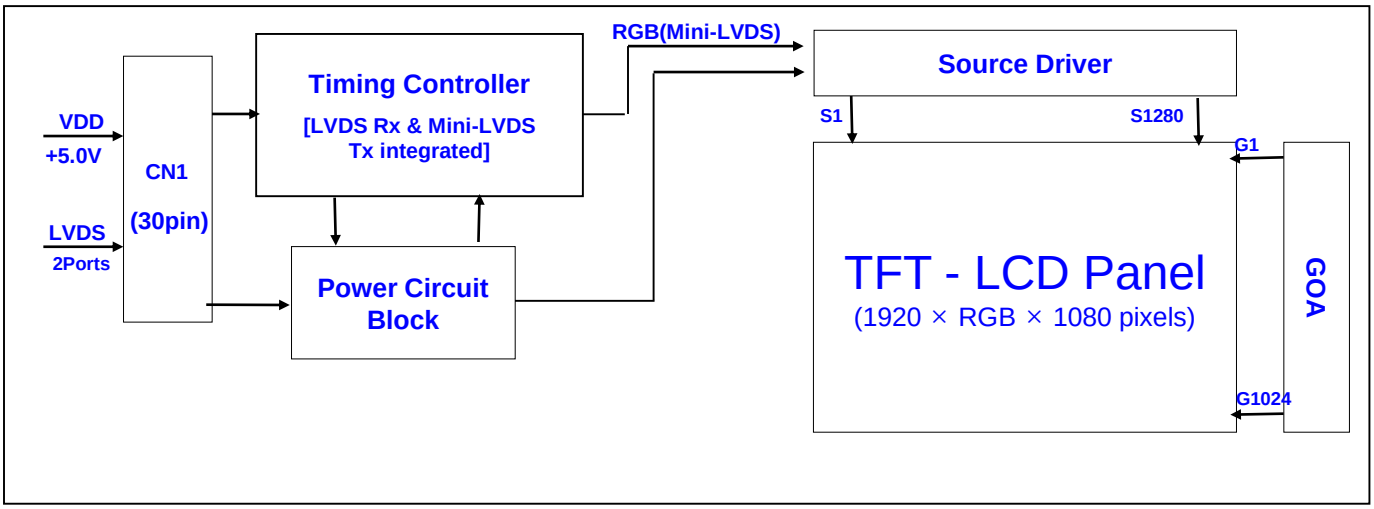
Revision No.	*Page*	*Description of changes*	*Date*	*Prepared*
P0		***Initial Release***	***2020.11.05***	

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

QV185FHB-N81 is a color active matrix TFT LCD MDL using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This Open Cell has a 18.5 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors

  Wide viewing angle

  DE (Data Enable) only mode

  HADS technology is applied for high display quality

  RoHS compliant

1.3 Application

- Commercial Digital Display
- Display Terminals for Control System
- Landscape and Portrait Display

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remarks
Active area	408.96 (H) × 230.04 (V)	mm	
Number of pixels	1920(H) ×1080(V)	pixels	
Pixel pitch	213(H) ×213(V)	um	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M	colors	Real 8bits
Display mode	Normally Black		
Dimensional outline	430.4(H) ×254.6(V)×0.8(D)	mm	Detail refer to drawing
Weight	TBD	g	
Sealing Area	6.69/5/6.62/6.62	mm	U/D/L/R
Surface Treatment	Haze 25%		

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	6.0	V	Ta = 25 ℃
Logic Supply Voltage	VIN	VSS-0.3	VDD+0.3	V	
Operating Temperature	T_{OP}	0	+50	℃	Note 1
Storage Temperature	T_{SUR}	-20	+60	℃	
	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

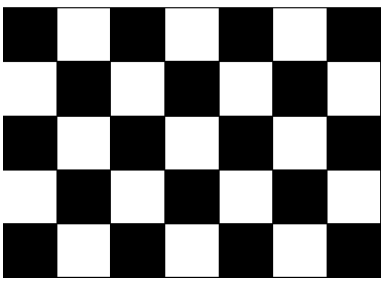
< Table 3. Open Cell Electrical Specifications >

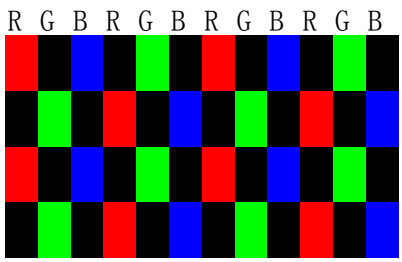
[Ta =25±2 ℃]

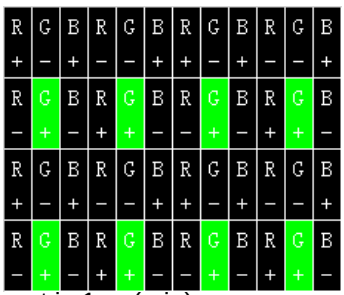
Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	4.5	5.0	5.5	Vdc	
Power Supply Ripple Voltage		VRP	-	-	200	mV	
Power Supply Current		IDD	-	400	1000	mA	Note 1
Power Consumption		PDD	-	2	5	Watt	
Rush current		IRUSH	-		3.0	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100	-	+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300	-	-100	mV	
	Input Differential Voltage	| VID |	200	-	600	mV	
	Differential input common mode voltage	VCM	1.0	1.2	1.5	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=5.0V,
Frame rate f_V=60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current

a) Typ : Mosaic 7X5 (L0/L255) b) Max : Skip 1 dot Pattern c) Flicker Pattern







Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

4.0 INTERFACE CONNECTION

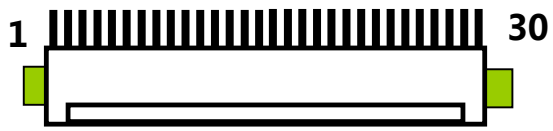
4.1 Open Cell Input Signal & Power （CN101）

- LVDS Connector : IS100-L30O-C23(UJU), MSBKT2407P30HC(STM) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	RXO0-	Negative Transmission data of Pixel 0 (ODD)	16	RXE1+	Positive Transmission data of Pixel 1 (EVEN)
2	RXO0+	Positive Transmission data of Pixel 0 (ODD)	17	GNG	Power Ground
3	RXO1-	Negative Transmission data of Pixel 1 (ODD)	18	RXE2-	Negative Transmission data of Pixel 2 (EVEN)
4	RXO1+	Positive Transmission data of Pixel 1 (ODD)	19	RXE2+	Positive Transmission data of Pixel 2 (EVEN)
5	RXO2-	Negative Transmission data of Pixel 2 (ODD)	20	RXEC-	Negative Transmission Cloc k (EVEN)
6	RXO2+	Positive Transmission data of Pixel 2 (ODD)	21	RXEC+	Positive Transmission Clock (EVEN)
7	GND	Power Ground	22	RXE3-	Negative Transmission data of Pixel 3 (EVEN)
8	RXOC-	Negative Transmission Clock (ODD)	23	RXE3+	Positive Transmission data of Pixel 3 (EVEN)
9	RXOC+	Positive Transmission Clock (ODD)	24	GND	Power Ground
10	RXO3-	Negative Transmission data of Pixel 3 (ODD)	25	NC	No. Connection
11	RXO3+	Positive Transmission data of Pixel 3 (ODD)	26	NC	No. Connection
12	RXE0-	Negative Transmission data of Pixel 0 (EVEN)	27	NC	No. Connection
13	RXE0+	Positive Transmission data of Pixel 0 (EVEN)	28	VDD	Power Supply: +5V
14	GND	Power Ground	29	VDD	
15	RXE1-	Negative Transmission data of Pixel 1 (EVEN)	30	VDD	

Note : Pin 24 should be connected with GND.

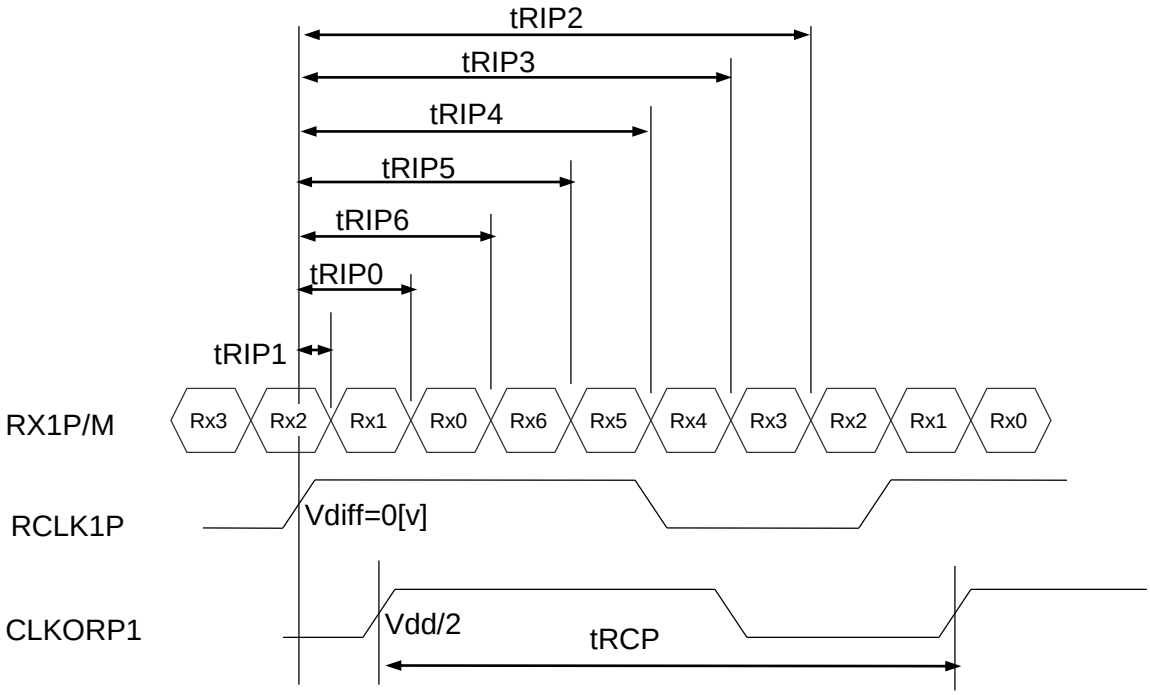


4.2 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 6. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	14.8	18.5	22.2	nsec	
Receiver Data Input Margin	tRMG	-0.35	-	0.35	nsec	fCLKIN=110MHz
		-0.40	-	0.40	nsec	fCLKIN=95MHz
		-0.45	-	0.45	nsec	fCLKIN=85MHz
		-0.60	-	0.60	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	-|tRMG|	0.0	|tRMG|	Clock	
Input Data 1	tRIP0	T/7-|tRMG|	T/7	T/7+|tRMG|	Clock	
Input Data 2	tRIP6	2 T/7-|tRMG|	2T/7	2T/7+|tRMG|	Clock	
Input Data 3	tRIP5	3T/7-|tRMG|	3T/7	3T/7+|tRMG|	Clock	
Input Data 4	tRIP4	4T/7-|tRMG|	4T/7	4T/7+|tRMG|	Clock	
Input Data 5	tRIP3	5T/7-|tRMG|	5T/7	5T/7+|tRMG|	Clock	
Input Data 6	tRIP2	6T/7-|tRMG|	6T/7	6T/7+|tRMG|	Clock	



* Vdiff = (RXz+)-(RXz-),…. ,(RXCLK+)-(RXCLK-)

5.0 SIGNAL TIMING SPECIFICATION

5.1 Timing Parameters (DE only mode)

< Table 8. Timing Table >

Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		60	74.25	78	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	3/7Tc	-	
Frame Period		Tv		1100	1125	1149	lines
				48.5	60	63	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1149	t_{HP}

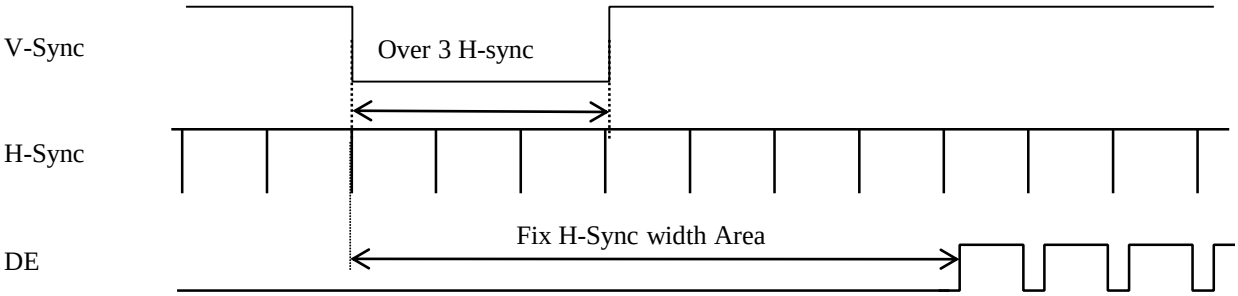
Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal op eration.

< Table 9. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	60	74.25	78	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±400mV	-380	-	+380	ps
F_{LVMOD}	Modulating frequency of input cl ock during SSC		60	-	85	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	100	ps

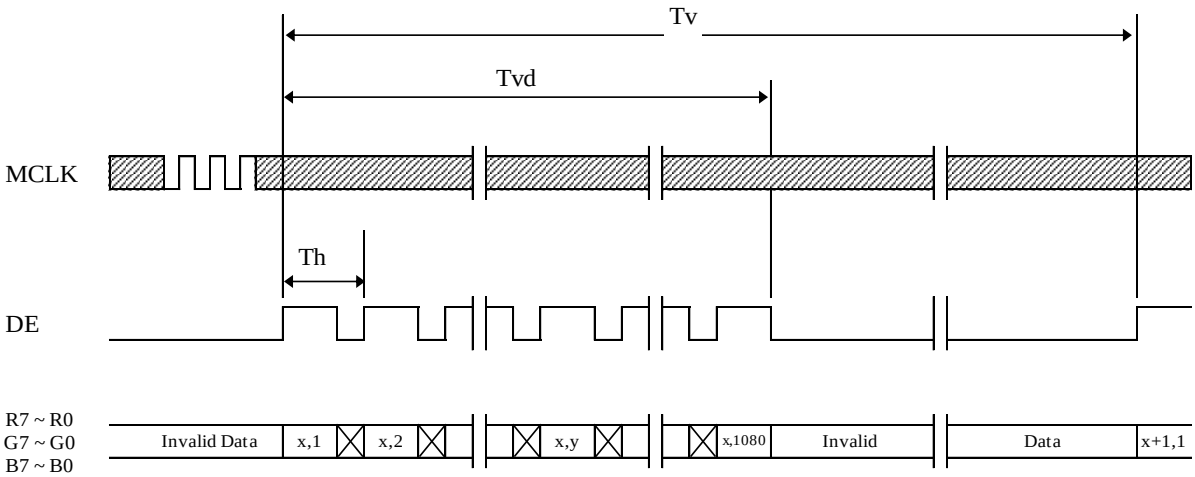
5.2 Signal Timing Waveform

5.2.1 Sync Timing Waveforms

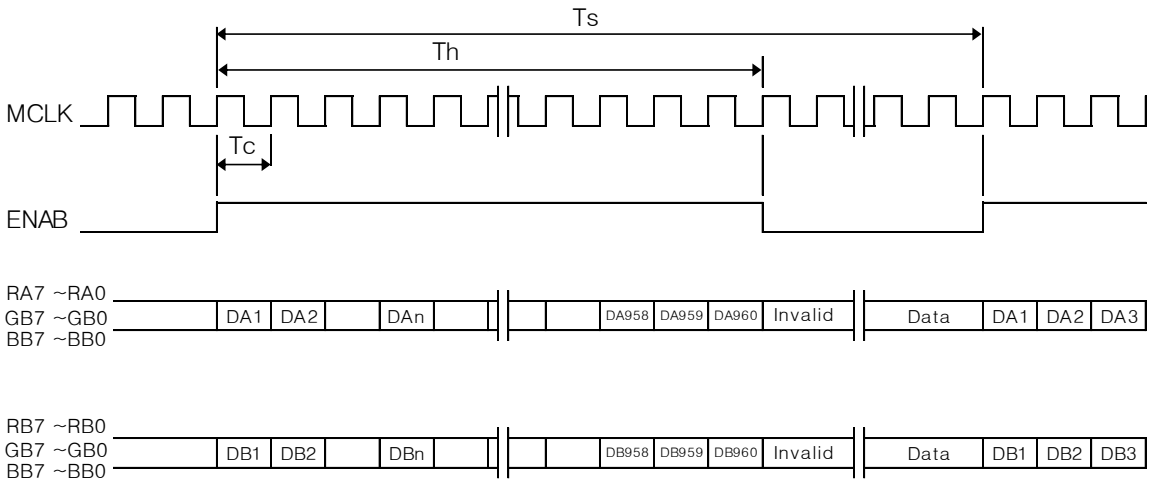


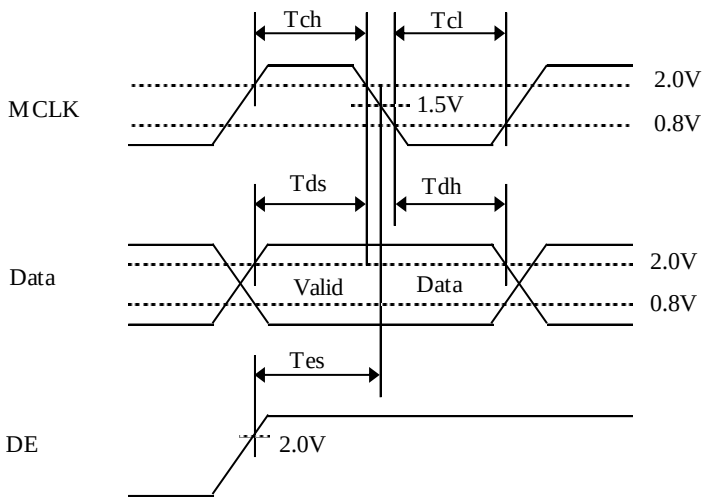
1) Need over 3 H-sync during V-Sync Low
2) Fix H-Sync width from V-Sync falling edge to first rising edge

5.2.2 Vertical Timing Waveforms



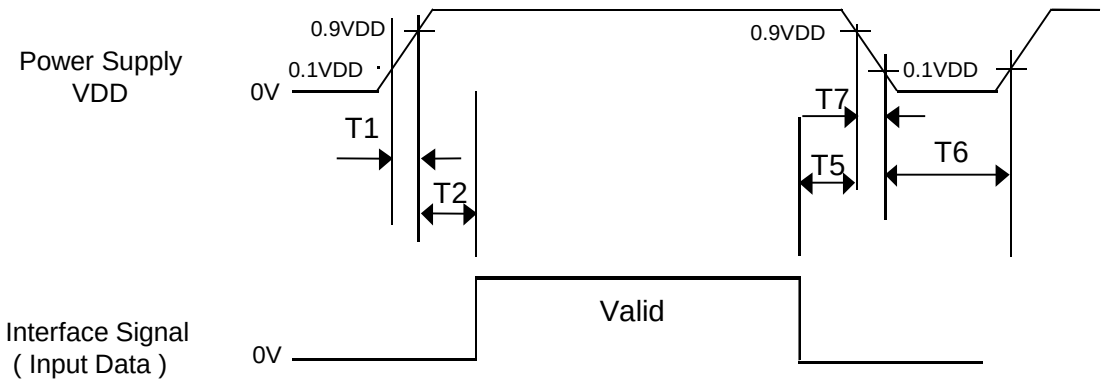
5.2.3 Horizontal Timing Waveforms





5.3 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall b e as shown in below



< Table 11. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	100	ms
T3	200	-	-	ms
T4	200	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.
3. When VDD<0.9VDD(Typ.),Power off.
4. T7 decreases smoothly, if there were rebounding voltage, it must smaller than 5 volts.

6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance 1 lux and temperature=25 2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0 . We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V at 25 C. Optimum viewing angle direction is 6 'clock.

< Table 12. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10	80	89	-	Deg.	Note 1
		Θ_9		80	89	-	Deg.	
	Vertical	Θ_{12}		80	89	-	Deg.	
		Θ_6		80	89	-	Deg.	
Brightness		Lv	Θ = 0 (Center) Normal Viewing Angle	200	250	-	nit	
Contrast ratio		CR		700:1	1000:1	-		Note 2
White luminance uniformity		ΔY		75	80	-	%	Note 3
Reproduction of color	White	W_x		TYP. - 0.03	TBD	TYP. + 0.03		Note 4
		W_y			TBD			
	Red	R_x			TBD			
		R_y			TBD			
	Green	G_x			TBD			
		G_y			TBD			
	Blue	B_x			TBD			
		B_y			TBD			
Color Gamut				68	72	-	%	
Cell Transmittance				TBD	TBD			
Response Time	G to G	T_g		-	14	20	ms	Note 5

17 . BACKLIGHT UNIT

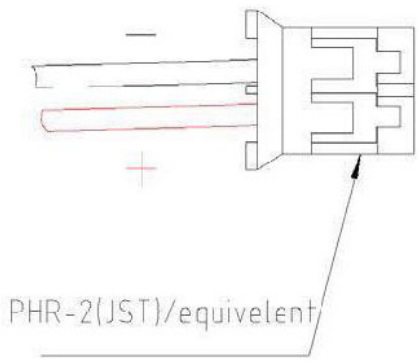
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Input Voltage Per Input Pin	VPIN	34	38	39	V	(1), Duty=100%, IPIN=(60mA)
灯条总电流I	IPIN	---	240	240	mA	(1), (2) Duty=100%
LED Life Time	LLED	**30000**			Hrs	(3)
Power Consumption	PBL	8.64	- - -	- - -	W	(1) Duty=100%, IPIN=(60mA)

Note (1) LED light bar input voltage and current are measured by utilizing a true RMS multimeter as shown below:

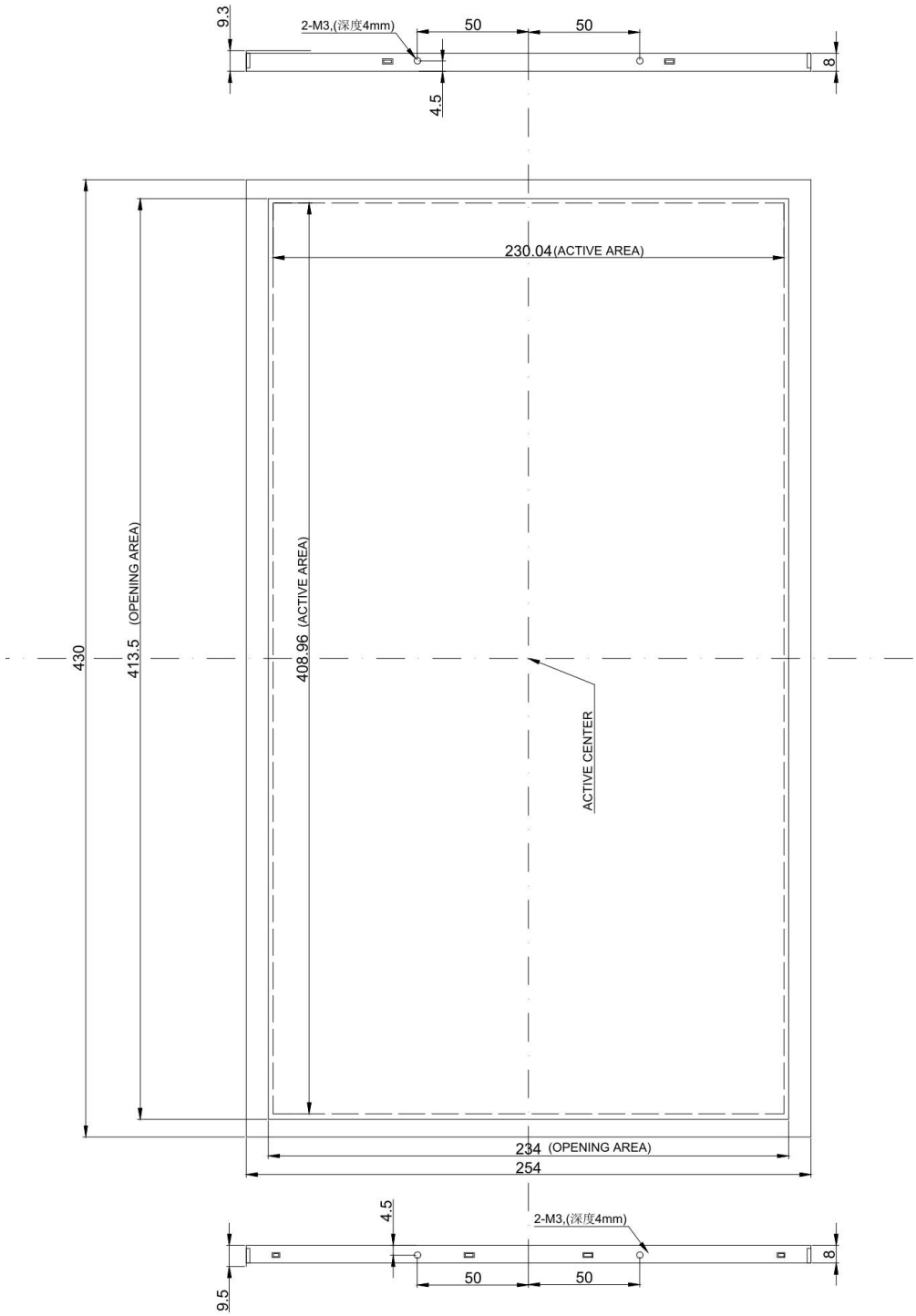
Note (2) PBL = IPIN × VPIN

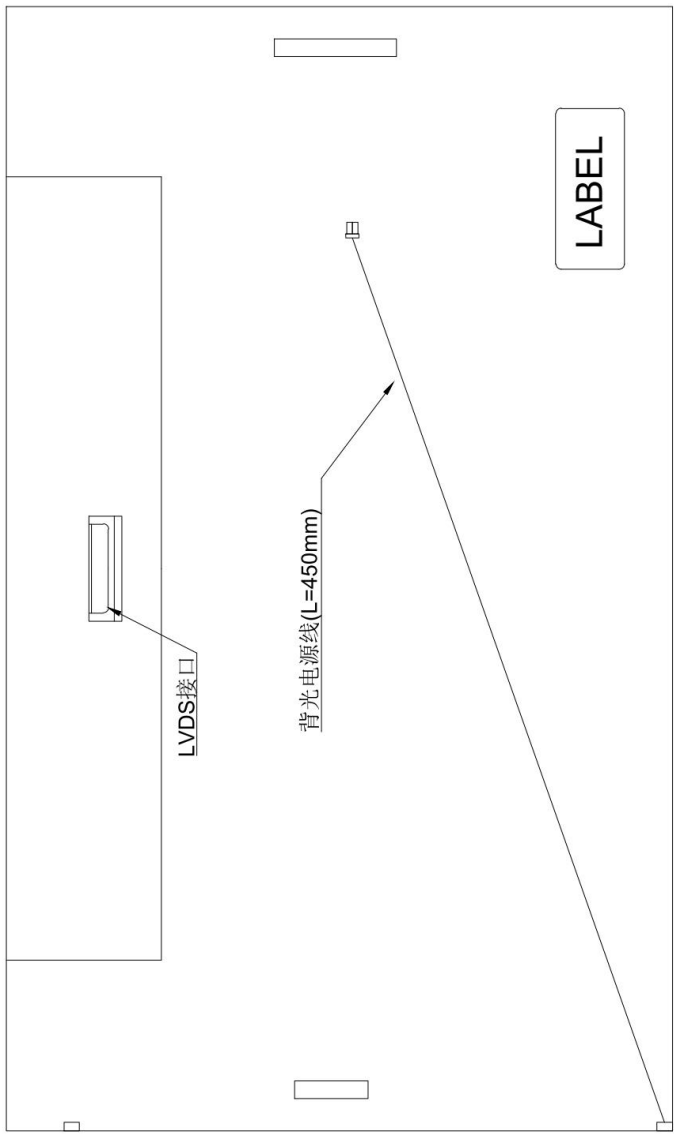
Note (3) The lifetime of LED is defined as the time when LED packages continue to operate under the conditions at Ta = 25 ±2 ℃ and I= (25)mA (per chip) until the brightness becomes ≦ 50% of its original value.

灯条串并定义及接口型号定义：4014（60MA）灯珠13串4并



7.0 2D Drawing




LABEL
背光电源线(L=450mm)
LVDS接口