Model name: PN215CT01-1

Date: 28. Sep. 2020

(√) Preliminary Specification

( ) Final Specification

Any modification is not allowed without HKC's permission

Customer's Approval	Chongqing HKC
Approved by Company(公司)：_____ Title(职称): _____ Signature(签名): _____	Approved By Product Director Date Name: Brain Signature:
	Reviewed By PM Manager Date Name: Lucius Signature:
Note	Reviewed By Project Leader Date Name: Wenxin Signature:
	Reviewed By PM Date Name: Yulin Signature:

Content

Revision History

Version	Date	Page (New)	Section	Description	Revision by
P1	2020/9/28	27	All	Preliminary Specification was First Issued.	Yulin

1. GENERAL DESCRIPTION

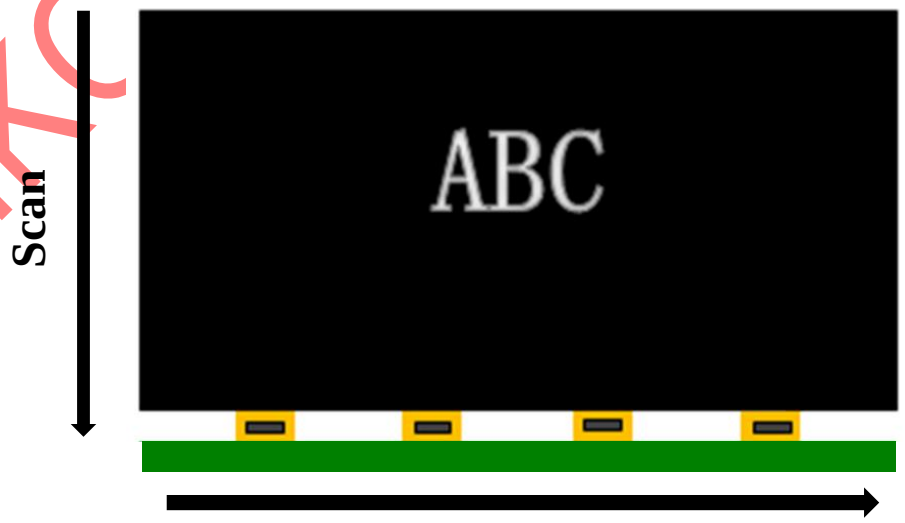
The specification is applied to 21.5” model (PN215CT01-1) TFT Liquid Crystal Display open cell and it supports 1920 x 1080 FHD mode with 16.7M (8bit) colors. This product is with driver ICs and a 30-pins-2ch-LVDS circuit board and built in without backlight unit.

1.1 General Specifications

Item	Specification	Unit	Note
Screen Size	21.5 inch Diagonal	mm	
Outline Dimension	487.44(H)x 278.182(V)	mm	D: cell thickness
Active area	476.64(H) x 268.11(V)	mm	-
Driver Element	a-Si TFT active matrix	-	-
Cell transmittance	5.1% (Typ.)	-	HKC BLU，center point
Pixel Number	1920 x 1080	pixel	-
Sub Pixel Pitch	0.08275(H) x 0.24825 (V)	mm	-
Pixel Arrangement	RGB Vertical	-	-
Display Colors	16.7M	color	8bit
Display Mode	Normally Black	-	-
Display Orientation	Signal input with“ABC”	-	-
Surface Treatment	Type=AG	-	-
	Haze=25%	-	-
	Top Surface Hardness : 3H	-	-
Weight	TBD	g	-

Note:

Fig. 1.1 Display Orientation



2. ABSOLUTE MAXIMUM RATINGS

2.1 Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause damage to the unit.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	6	V	(1)
Input Signal Voltage	V_{in}	-0.3	3.6	V	(1)

Note:

(1) Within Ta=25±2℃

2.2 Absolute Ratings of Environment

Temperature and relative humidity range are shown as below.

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	℃	(1)
Operating Temperature	TOP	0	50	℃	(1), (2)
Panel Surface Temperature of Display Area	PST	-	65	℃	(3)

Note:

(1) a. 90 % RH Max. (Ta ≤ 40 °C).

b. Web-bulb temperature should be 39℃ Max.(Ta>40℃)

c. No condensation

d. Operating condition with a assemble module

(2) Any point on the Driver surface must be less than 120 ℃ under any condition ,If the surface temperature is out of the spec, thermal solutions should be applied to avoid be damaged.

(3) Surface temperature of display area is measured at 50 ℃ dry condition.

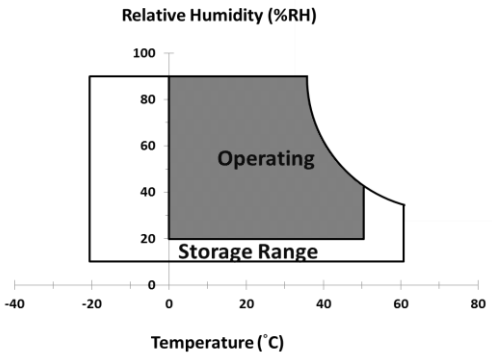


Fig. 2.1 Operating and storage environment

2.3 Package Storage

When storing open cell as spares for a long time, please follow the precaution instructions:

(1) Do not store the open cell in high temperature and high humidity for a long time. It is highly recommended to store the module with temperature from 20℃ to 30℃ in normal humidity (50 ±10%RH) with shipping package.

(2) The open cell should be keep within one month shelf life.

3. ELECTRICAL SPECIFICATIONS

3.1 Electrical Characteristics

3.1.1 Power Consumption

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5	5.5	V	(2)
Rush Current		I_{RUSH}	-	-	(3)	A	(3)
Power Supply Current	White Pattern	Icc	-	(0.8)	(1.04)	A	(4)
	Horizontal Stripe	Icc	-	(1.28)	(1.66)	A	
	Black Pattern	Icc	-	(0.78)	(1.01)	A	
Power Consumption		P_{LCD}		(4)	(5.2)	Watt	White Pattern

Note:

(1) Ambient temperature: 25 ±2℃

(2) The ripple voltage should be controlled less than 10% of V_{CC}.

(3) Measurement condition: V_{CC} rising time = 470μs.

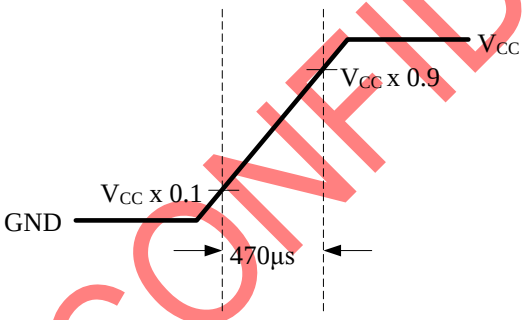
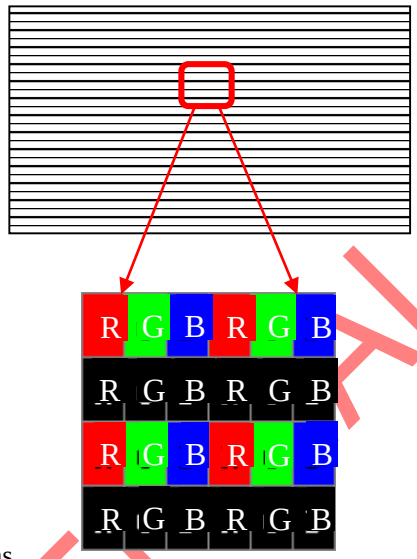


Fig. 3.1 V_{CC} rising time condition

(4) Measurement condition: V_{CC} = 5.0, Ta = 25 ±2 ℃, F = 60 Hz. The test patterns are shown as below.

A. White Pattern

B. Horizontal Pattern



C. Black Pattern

Fig. 3.2 Test patterns

3.1.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	80	100	120	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

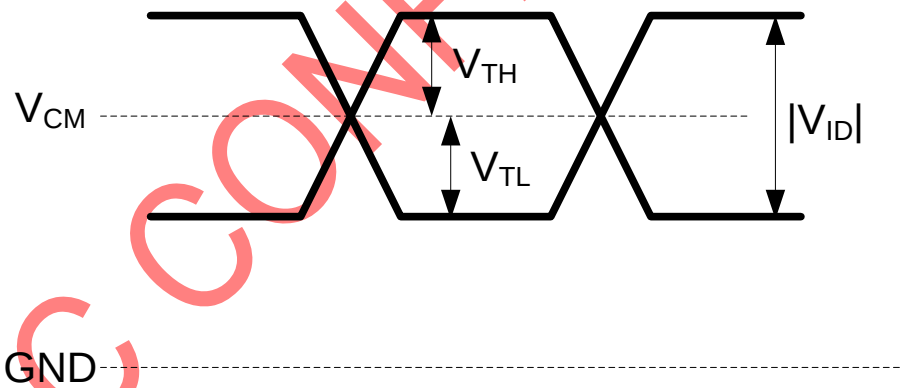


Fig. 3.3 LVDS Input signal

3.1.3 LVDS Format

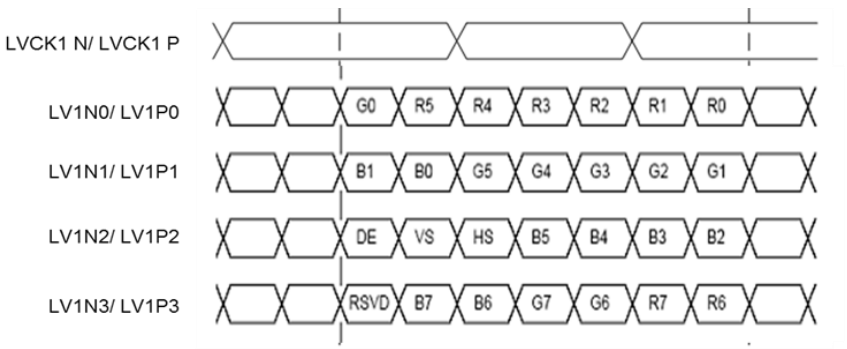


Fig. 3.4 VESA format

3.2 Interface Connections

Interface Pin Assignment

CN1: 3-10122314-0 (XDYT) or equivalent 1mm pitch 30 pin (1)

Pin No.	Symbol	Description	Note
1	ORX0N	LVDS Data1(0) -	
2	ORX0P	LVDS Data1(0) +	
3	ORX1N	LVDS Data1(1) -	
4	ORX1P	LVDS Data1(1) +	
5	ORX2N	LVDS Data2(2) -	
6	ORX2P	LVDS Data2(2) +	
7	GND	Power Ground	
8	ORXCN	LVDS clock1 -	
9	ORXCP	LVDS clock 1+	
10	ORX3N	LVDS Data1(3) -	
11	ORX3P	LVDS Data1(3) +	
12	ERX0N	LVDS Data2(0) -	
13	ERX0P	LVDS Data2(0) +	
14	GND	Power Ground	
15	ERX1N	LVDS Data2(1) -	
16	ERX1P	LVDS Data2(1) +	
17	GND	Power Ground	
18	ERX2N	LVDS Data2(2) -	
19	ERX2P	LVDS Data2(2) +	
20	ERXCN	LVDS clock2 -	
21	ERXCP	LVDS clock 2+	
22	ERX3N	LVDS Data2(3) -	
23	ERX3P	LVDS Data2(3) +	
24	NC	No Connection	(2)
25	NC	No Connection	(2)
26	NC	No Connection	(2)
27	NC	No Connection	(2)
28	VIN5	Power supply +5.0V	
29	VIN5	Power supply +5.0V	
30	VIN5	Power supply +5.0V	

Note:

(1) Following finger shows the LVDS pin1 diagram.

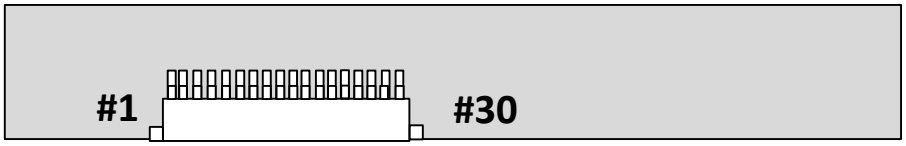
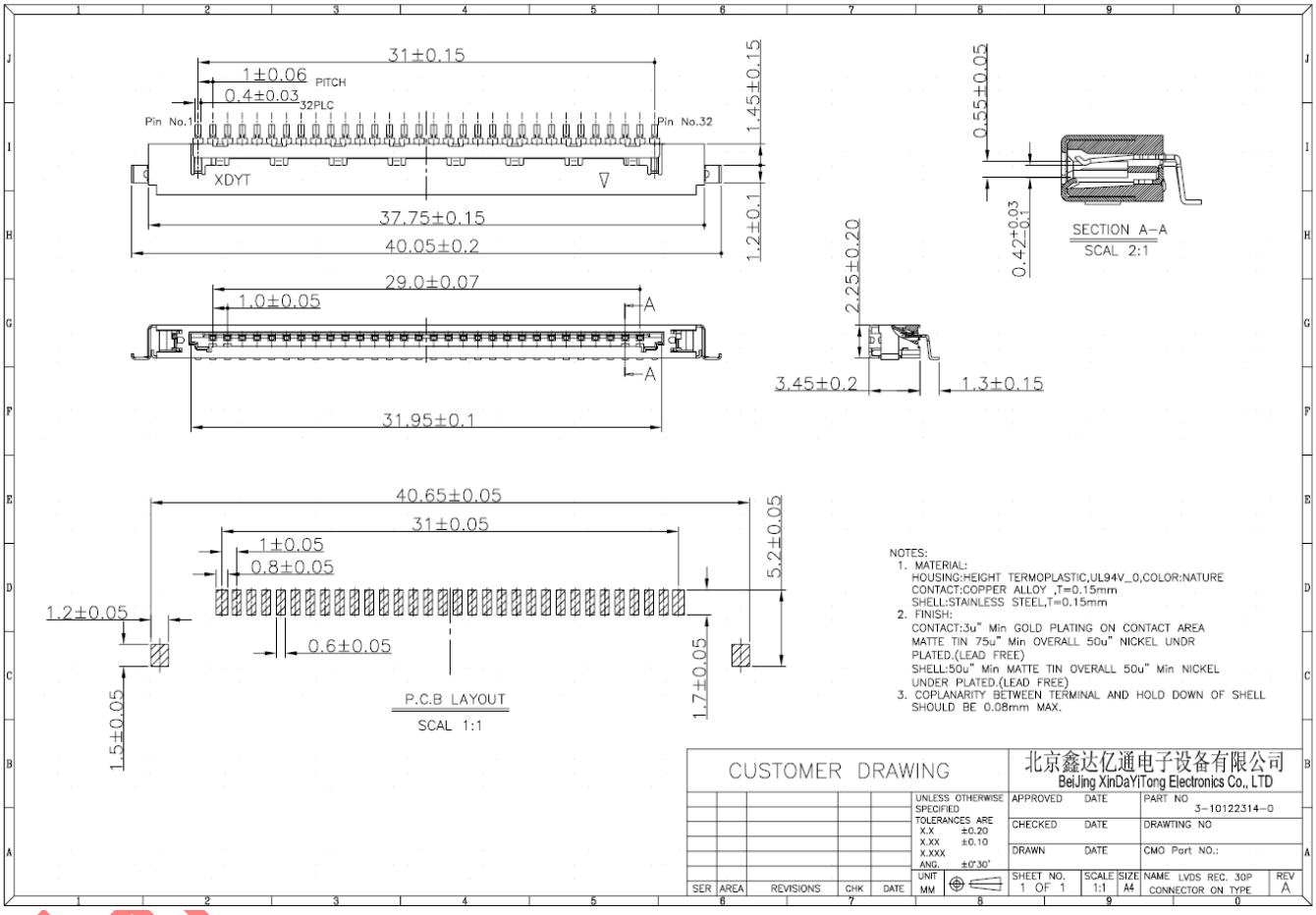


Fig. 3.5 LVDS connector direction sketch map

(2) For HKC used only, please leave it open.

Connector Drawing



3.3 Timing Spec

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_{clkin}	50	74.25	90	MHz	(1)
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(2)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	(3)
	Spread spectrum modulation frequency	FSSM	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-400	-	400	ps	(4)
Vertical Term	Frame Rate	**F**	48	60	76	Hz	
	Total	**T_V**	1094	1125	1836	T_H	$T_V = T_{VD} + T_{VB}$
	Active Display	**T_{VD}**	1080			T_H	
	Blank	**T_{VB}**	14	45	756	T_H	
Horizontal Term	Total	**T_H**	1050	1100	1678	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Active Display	**T_{HD}**	960			T_{CLK}	
	Blank	**T_{HB}**	90	140	718	T_{CLK}	

Attention:

The module is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

Note:

(1) Please make sure the range of pixel clock follows the following equations:

$Fclkin(max) \geq Fmax \times Tv \times T_H$

$Fmin \times Tv \times T_H \geq Fclkin(min)$

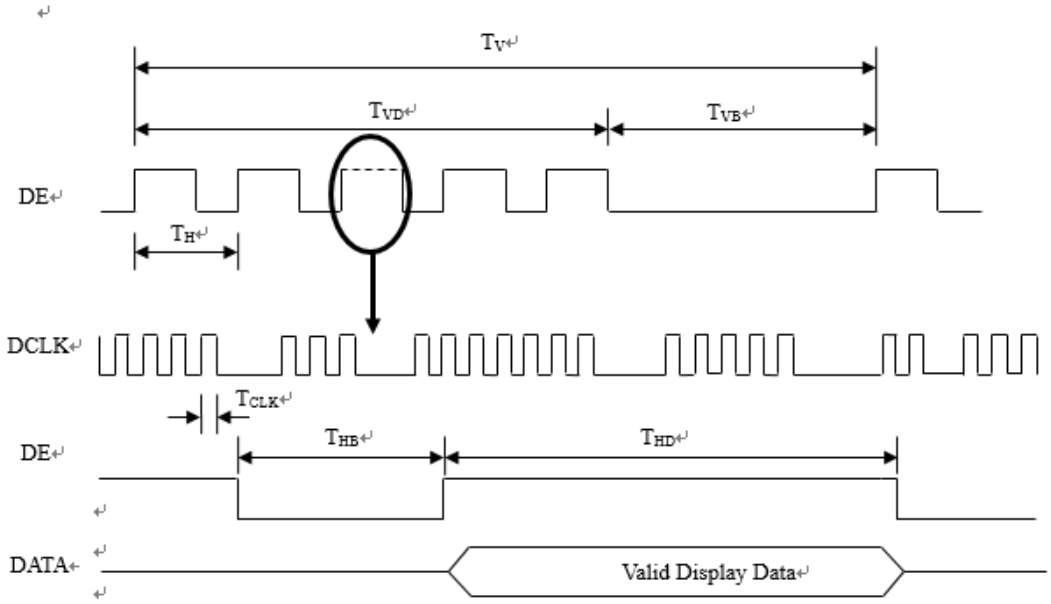
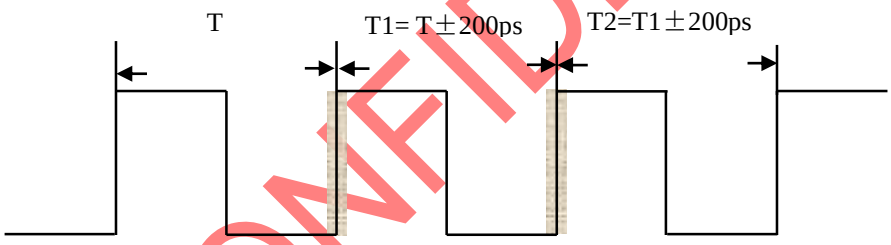


Fig 3.8 Signal timing diagram

(2)The input clock cycle-to-cycle is defined as below figures.



(2) The input clock cycle-to-cycle is defined as below figures.

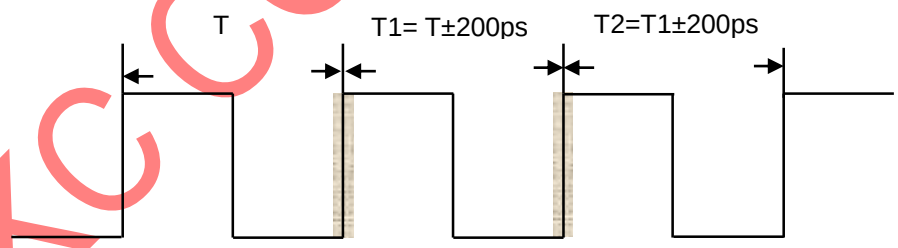


Fig. 3.7 Jitter

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure. The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

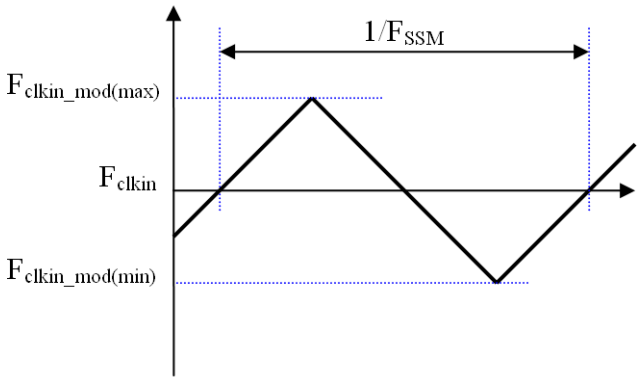


Fig. 3.8 SSCG

(4) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

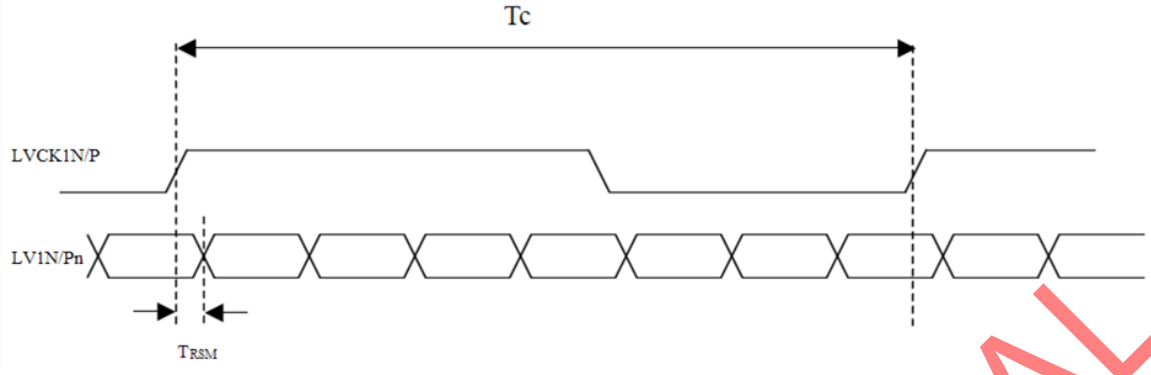


Fig. 3.9 LVDS receive interface timing diagram

3.4 Power On/Off Sequence

The power sequence specifications are shown as the following table and diagram.

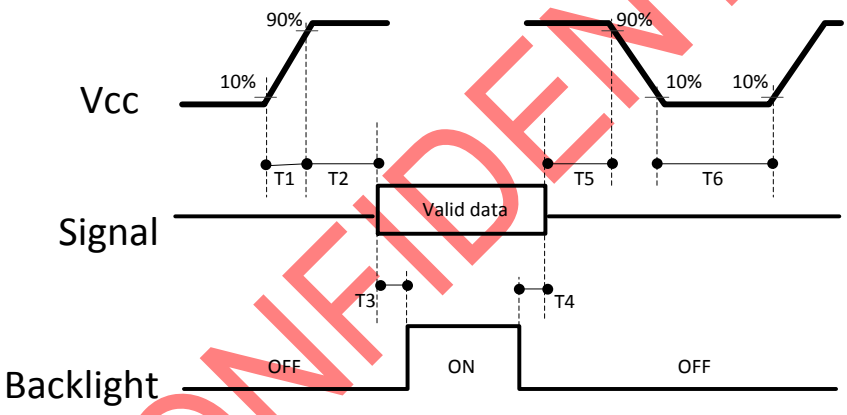


Fig. 3.10 Power on/off signal sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	500	-	-	ms
T4	100	-	-	ms
T5	0	-	50	ms
T6	1000	-	-	ms

Attention:

(1) The supply voltage of the external system for the module input should be the same as the definition.

(2) To avoid some abnormal display noise, we suggest " V_{CC}" falling time to follow "T6" definition.

(3) The product should be always operated within above ranges.

(4) In case of V_{CC} is off level, please keep the level of input signals on the low or keep high impedance.

3.5 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

sub pixel checker under 50% gray level.

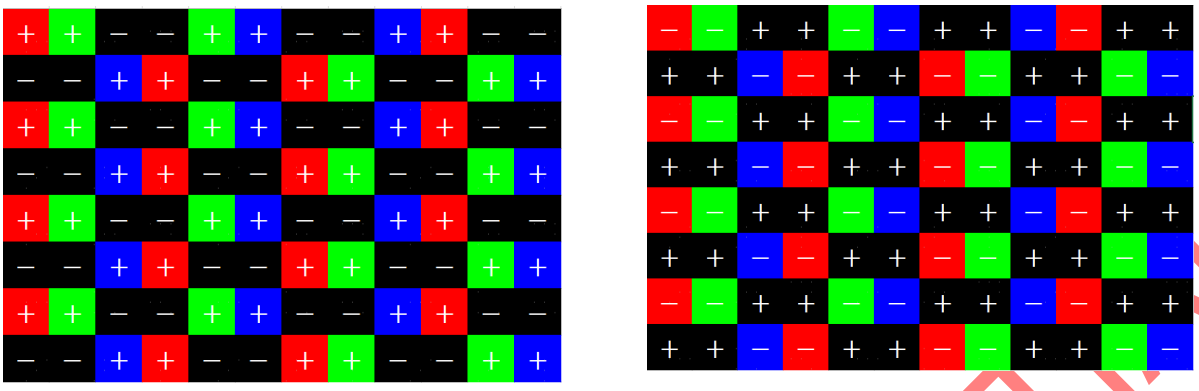


Fig. 3.11 Flicker pattern

3.6 Driver IC ESD Spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.12

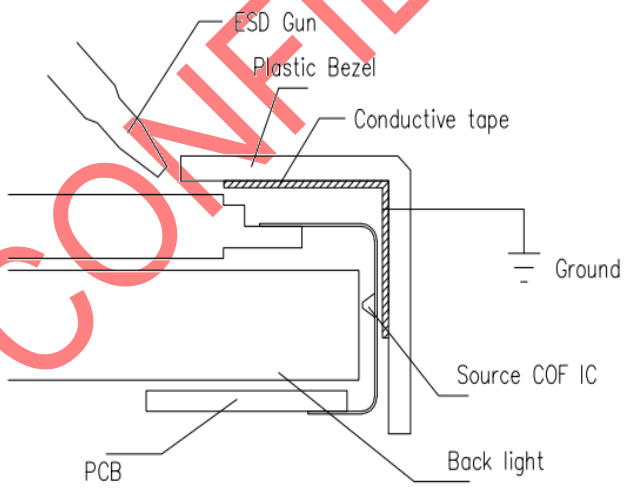


Fig. 3.12 Source COF IC ESD protection

4. OPTICAL CHARACTERISTICS

4.1 Measurement Conditions

The table below is the test condition of optical measurement.

Item	Symbol	Value	Unit
Ambient Temperature	T_A	25±2	℃
Ambient Humidity	H_A	50±10	% RH
Supply Voltage	V_{CC}	5	V
Driving Signal	Refer to the typical value in Chapter 3: Electrical Specification		
Vertical Refresh Rate	F_v	60	Hz
Light source	HKC module White LED Backlight Module/ Film structure		
Warm up time	Twarm	>30 min	min
Dark room	ED	1lux>	lux

To avoid abrupt temperature change during optical measurement, the measurement should be executed in a stable, windless, in dark room after lighting the light source, and the measurement position is the center of the panel.

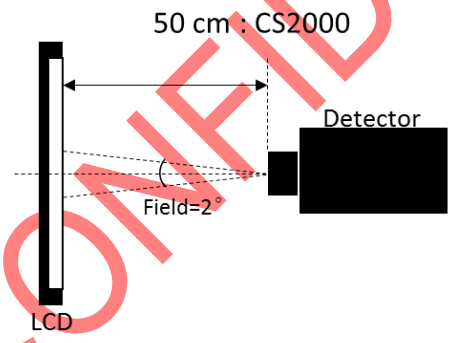


Fig. 4.1 Measurement equipment

4.2 Optical Specifications

The relative measurement methods of optical characteristics are shown in 4.2. The following items should be measured under the test conditions described in 4.1 and stable environment shown in 4.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE1931)	Red	Rx	θ_x=0°,θ_y=0° Viewing Angle at Normal Direction at center point of panel, Light source is HKC BLU	Typ.- 0.03	(0.638)	Typ.+ 0.03	-	(1)
		Ry			(0.331)			
	Green	Gx			(0.314)			
		Gy			(0.617)			
	Blue	Bx			(0.156)			
		By			(0.043)			
	White	Wx			(0.287)			
		Wy			(0.291)			
Color Gamut		CG		(68)	(72)	-	%	(2)
Transmittance		T%		(4.5)	(5.1)	-	%	(3)
Contrast Ratio		CR	θ_x=0°,θ_y=0° With HKC BLU	(2000)	(3000)	-	-	(4)
Response Time		T_g		-	(7.0)	(12)	ms	(5)
Viewing Angle	Horizontal	θ_x+	CR≧10 θ_x=0°,θ_y=0°	-	89	-	Deg.	(6)
		θ_x-		-	89	-		
	Vertical	θ_y+		-	89	-		
		θ_y-		-	89	-		

Note:

Light source here is the backlight of HKC BLU, and film structure is two diffuser sheets.

(1) Each chromaticity coordinates (x, y) are measured in CIE1931 color space when full-screen displaying (Red, Green, Blue, White) and light source is defined by HKC BLU, measurements shall be made at the center of the panel, and setup of measurement is shown in Fig. 4.1.

(2) The color gamut is defined as the fraction in percent of the area of the triangle bounded by R, G, B coordinates and the area is defined by NTSC 1931 color standard in the CIE color space. Chromaticity coordinates are measured by CS2000 and the standard setup of measurement is shown in Fig. 4.1.

(3) Definition of Transmittance (T%):

The transmittance is measured with full white pattern (L_{max}) at the center of the LCD panel.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}}$$

(4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression,

Contrast Ratio (CR): $\boldsymbol{CR} = \frac{\boldsymbol{CR_W}}{\boldsymbol{CR_D}}$

CR_W : Luminance of LCD module with full screen white pattern (255,255, 255) at center point.

CR_D : Luminance of LCD module with full screen Dark pattern (0, 0, 0) at center point.

Where the measure point of to the Contrast Ratio is the center of the panel

(5) Definition of Response time (Tg):

Average of gray to gray response time (T_g) means the average switching time of luminance ratios among 0%,25%,50%,75%,and 100% to each other and is optimized on frame rate =60Hz.

Measured Response time		To				
		0%	25%	50%	75%	100%
From	0%		$T_{0\%to25\%}$	$T_{0\% to 50\%}$	$T_{0\% to 75\%}$	$T_{0\% to 100\%}$
	25%	$T_{25\% to 0\%}$		$T_{25\% to 50\%}$	$T_{25\% to 75\%}$	$T_{25\% to 100\%}$
	50%	$T_{50\% to 0\%}$	$T_{50\% to 25\%}$		$T_{50\% to 75\%}$	$T_{50\% to 100\%}$
	75%	$T_{75\% to 0\%}$	$T_{75\% to 25\%}$	$T_{75\% to 50\%}$		$T_{75\% to 100\%}$
	100%	$T_{100\% to 0\%}$	$T_{100\% to 0\%}$	$T_{100\% to 50\%}$	$T_{100\% to 75\%}$	

Table. 4.2 Switching time of luminance ratios matrix

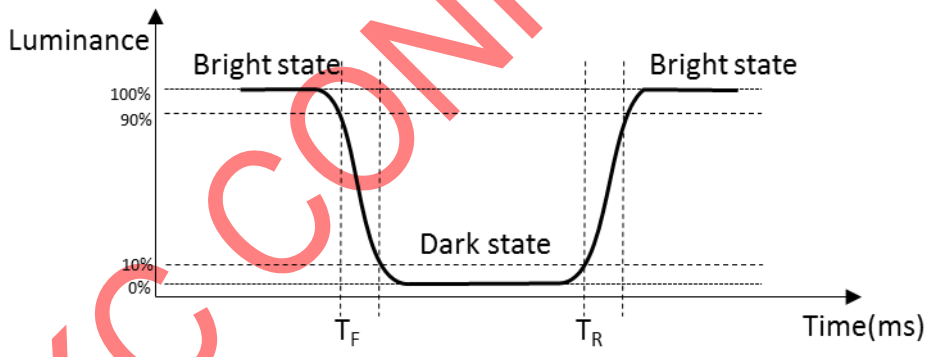


Fig. 4.3 The definition of T_R and T_F

Measured response time is determined by 10% to 90% brightness difference of rising (T_R) or falling (T_F) time.

(6) Definition of Viewing angle:

As Note (4) the static contrast ratio definition, the viewing angles are defined at the angle that the contrast ratio is larger than 10 at four directions relative to the perpendicular direction of the HKC's module (two vertical angles: up θ_y+ and down θ_y-; and two horizontal angles: right θ_x+ and left θ_x-). The standard setup of measurement is shown in Fig. 4.1 & 4.4

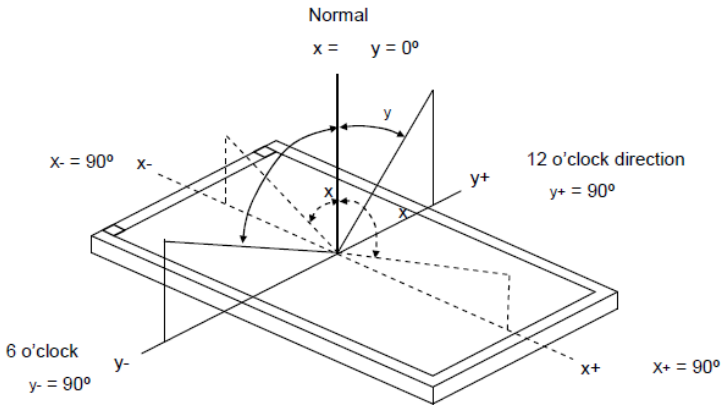
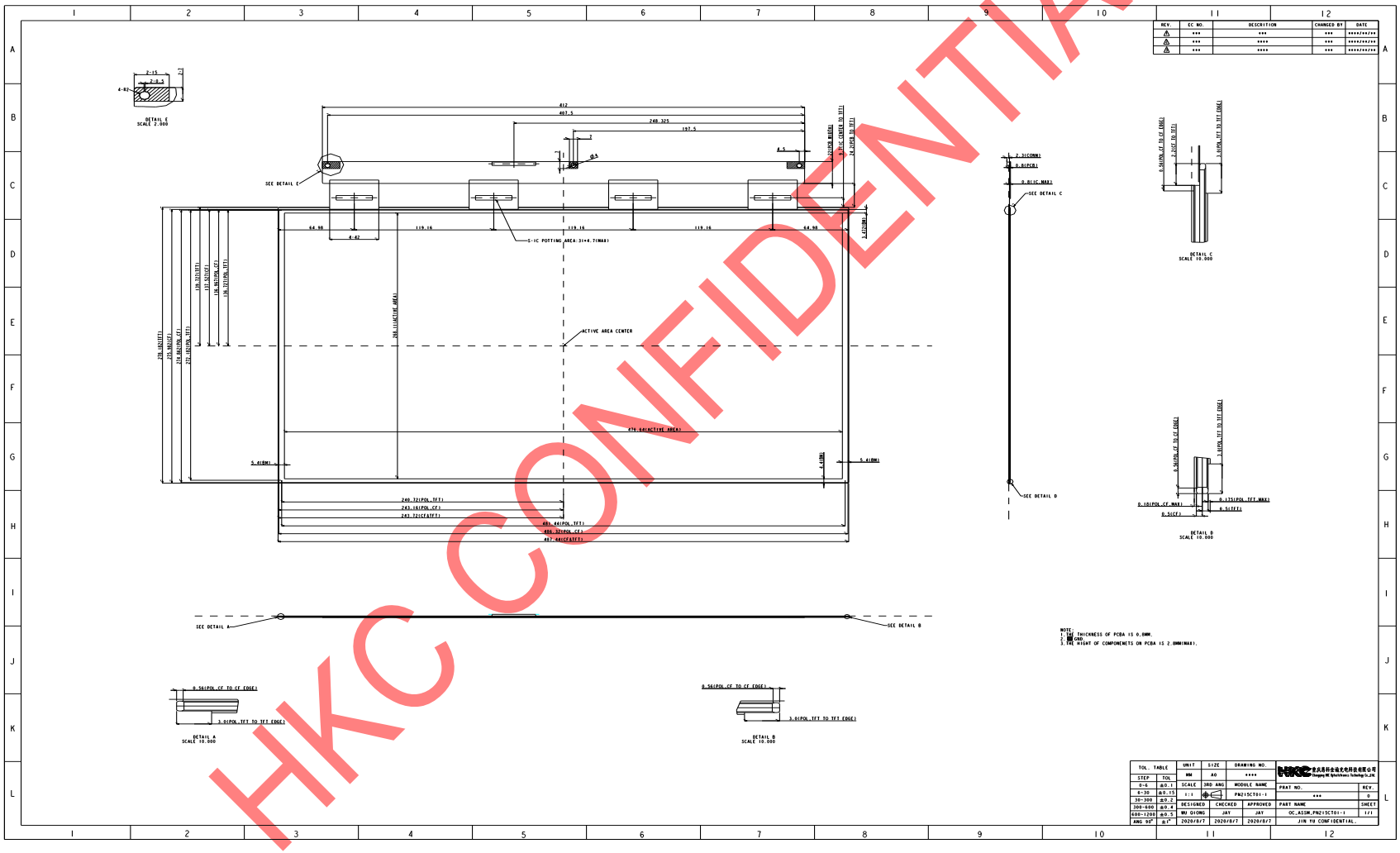


Fig. 4.4 View angle coordination system

5. MECHANICAL CHARACTERISTICS

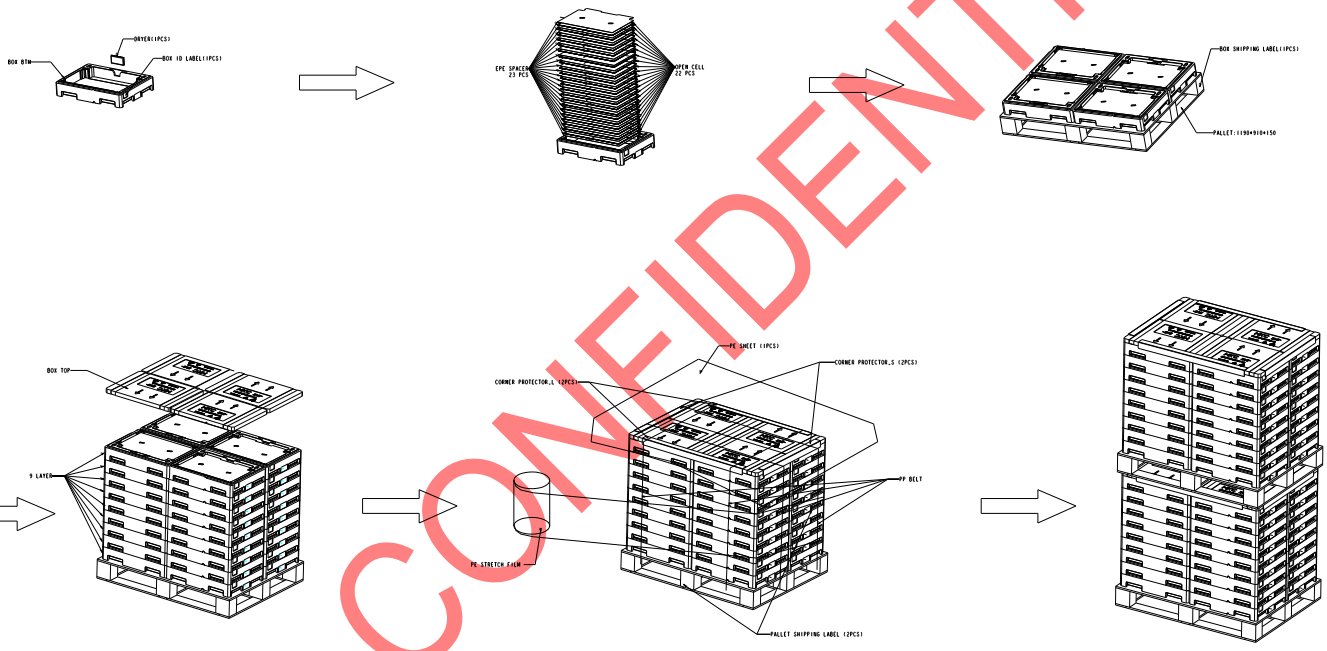
5.1 Mechanical Specification



5.2 Packing

5.2.1 Packing Specifications

Item	Specification			
	Quantity	Dimension(mm)	Item	Weight(Kg)
Packing Box	22 pcs/box	580(L) x 425(W) x 108(H)	Net Weight Gross Weight	9.02 9.61
Pallet	1	1190(L) x 910(W) x 150 (H)	Net Weight	16.5
Stack Layer	9			
Boxes per Pallet	36			
Pallet after Packing	792pcs/pallet	1190(L) x 910(W) x 1062(H)	Gross Weight	364



6. DEFINITION OF LABELS

6.1 Open Cell Label

XXXXXXXXXXXXXXXXXXXXX YMDD PN215CT01-1 Ver.X.X

- Version
- Model Name
- Year, Month,
- Serial Number

Serial Number : XXXXXXXXXXXX XXXXXXXXX

- HKC Internal Use
- Panel ID

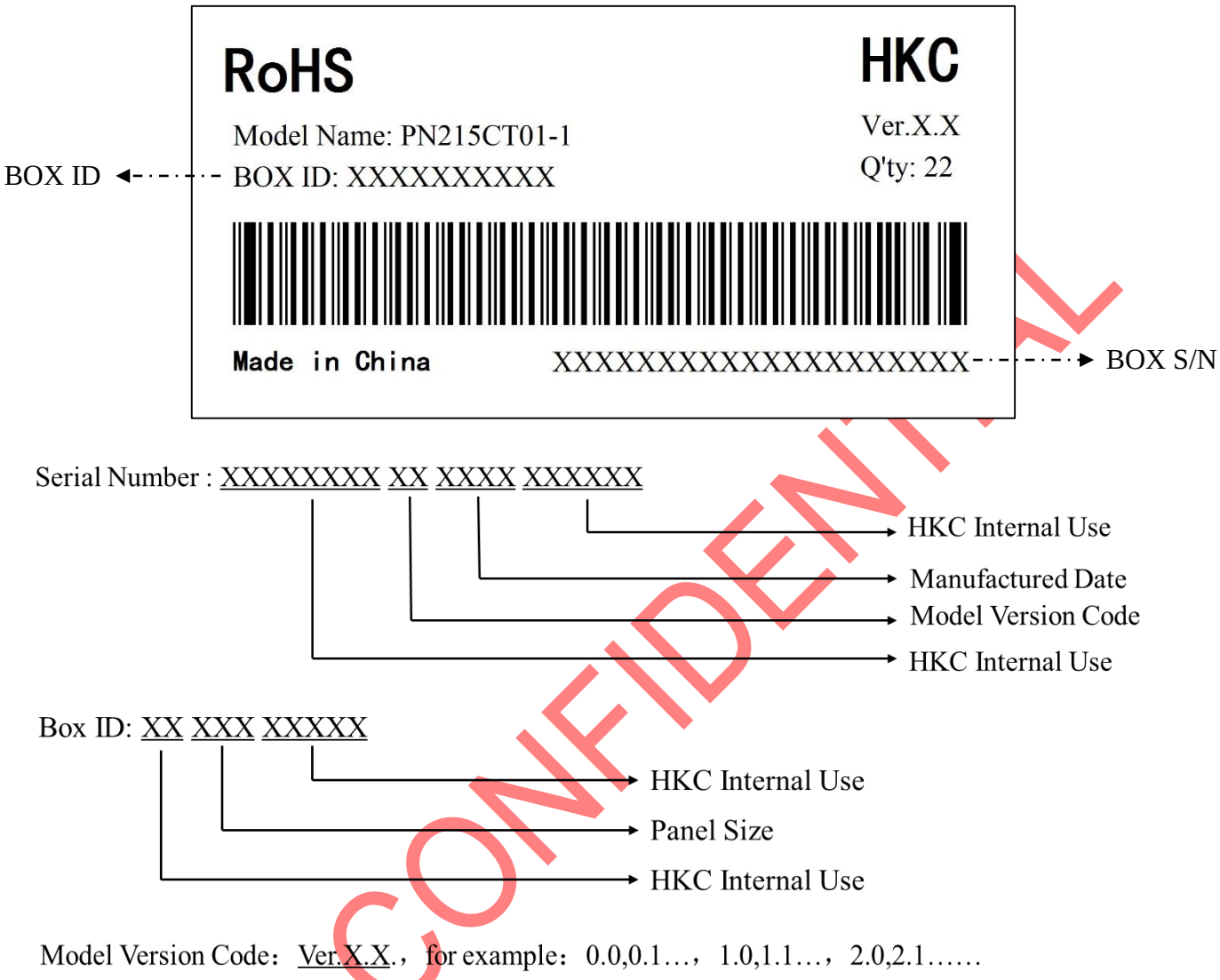
Manufactured Date: Y M DD

- Date:01~31
- Month: 1~9，A~C，for Jan ~Dec
- Year：2018=8，2019=9，2020=0

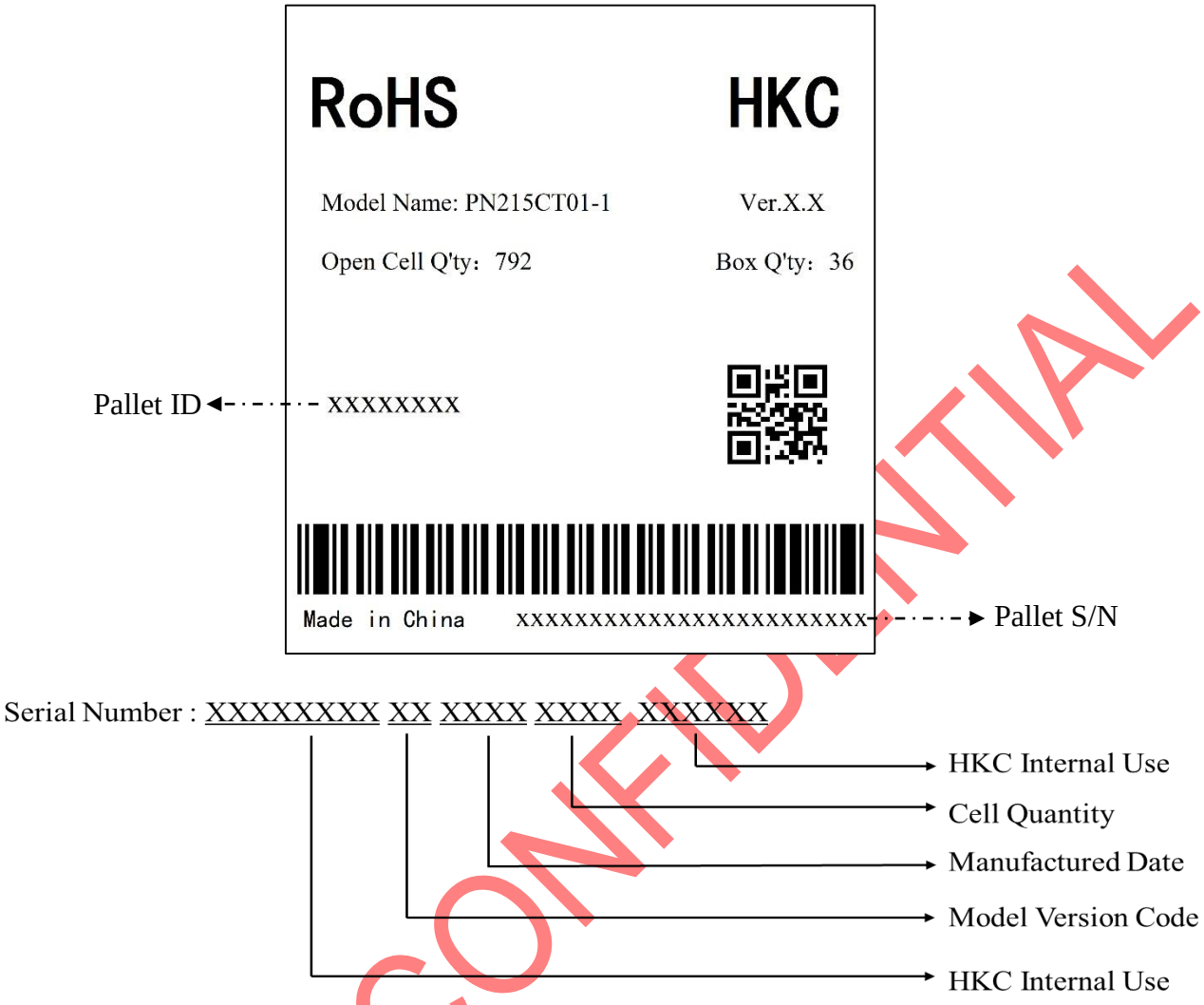
Model Name: PN215CT01-1

Model Version Code：Ver.X.X.，for example：0.0,0.1…，1.0,1.1…，2.0,2.1……

6.2 Carton Label



6.3 Pallet Label



7. PRECAUTION

Please pay attention to the followings when a TFT-LCD cell is used, handled and mounted.

7.1 Unpacking

Should use immediately after unpacking TFT -LCD cell to prevent the terminal corrosion.

Protection film for a polarizer on a TFT open cell should be slowly peeled off so that the electrostatic charge can be minimized.

Source PCB should be connected to the ground when peel off the protection film.

The protection film should not be contacted to the driver during peeling off.

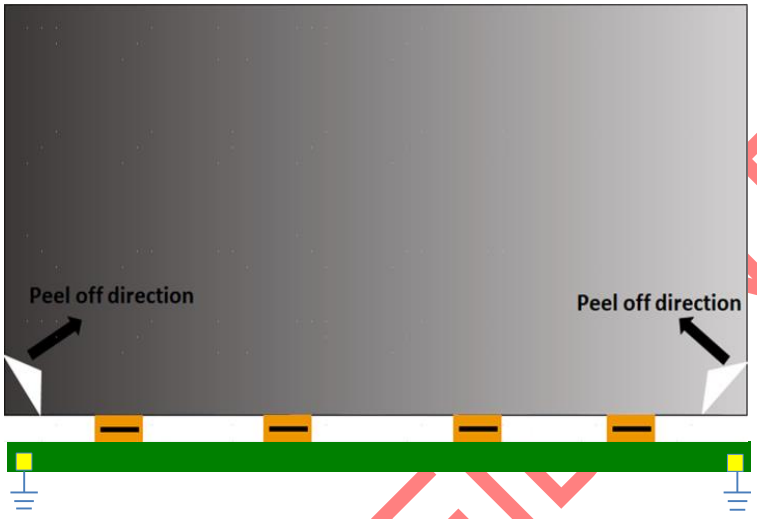


Fig 7.1 Unpacking

Please pay attention to side glass scratch when a TFT –LCD cell is used for floating display, as shown in Fig.7.2.

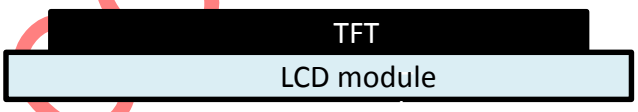


Fig 7.2 Floating display section

7.2 Storage Test

Any attachment on polarizer of open-cell, such as tape, is forbidden and not recommend, especially under the high temperature and high humidity environment.

8. GP REQUIREMENT

a) RoHS, Directive 2011/65/EU of the European Parliament and council of 1 July 2011

b) RoHS, Directive (EU) 2015/863 of the European Parliament and council of 31 March 2015

c) PPW